IN THE CLAIMS:

1. (Currently amended) Network node apparatus, comprising:

a physical layer interface (PHY) device, which comprises a network port and a data output port, and is adapted to receive signals from a communication network through the network port and to process the signals in accordance with a predetermined physical layer protocol so as to generate a digital data output at the data output port; and

a field-programmable logic device, comprising:

a configuration port, which is coupled to the data output port of the PHY device so as to receive program code, which is transmitted over the network during a programming phase in order to program the field-programmable logic device; and

a data input port, which is separate from the configuration port and is also coupled to the data output port of the PHY device so as to receive communication data transmitted over the network following conclusion of the programming phase, whereupon the field programmable logic device is programmed by the program code to process the communication data in accordance with a predetermined data link layer protocol.

2. (Previously presented) The apparatus according to claim 1, wherein the apparatus comprises no non-volatile memory for holding the program code.

3. (Previously presented) The apparatus according to claim 1, wherein the configuration port and data input port are connected in parallel to the data output port without other logic components intervening between the ports.

4. (Original) The apparatus according to claim 1, wherein the physical layer protocol and data link layer protocol comprise Ethernet protocols.

5. (Original) The apparatus according to claim 4, wherein the PHY device is adapted to generate the digital data output in accordance with an Ethernet media independent interface (MII).

6. (Original) The apparatus according to claim 1, wherein during the programming phase, the digital data output comprises a sequence of clock bits, which are generated by the PHY device responsively to the signals received from the communication network, and wherein the field programmable logic device comprises a clock input, which is coupled to receive the clock bits so as to clock the program code into the input port.

7. (Original) The apparatus according to claim 1, wherein the field programmable logic device further comprises a data transmit port and is further programmed by the program code to generate data frames at the data transmit port in accordance with the data link protocol, and

wherein the PHY device comprises a data receive port, which is coupled to the data transmit port so as to receive the data frames generated by the field programmable logic device for transmission over the communication network via the network port.

8. (Original) The apparatus according to claim 1, wherein the field programmable logic device comprises a field programmable gate array (FPGA).

9. (Original) The apparatus according to claim 1, and comprising an identification (ID) component holding an identification value and coupled to be read by the field programmable logic device, so that when the field programmable logic device is programmed by the program code, the field programmable logic device conveys the identification value over the network to a code server.

10. (Currently amended) Apparatus for communication over a network, which operates in accordance with a predetermined physical layer protocol, the apparatus comprising:

a code server, which is adapted to transmit program code over the network during a programming phase of the apparatus; and

a network node, comprising:

a physical layer interface (PHY) device, which comprises a network port and a data output port, and is adapted to receive signals from the network through the network port and to process the signals in accordance with the physical layer protocol so as to generate a digital data output at the data output port; and

a field-programmable logic device, comprising a configuration port, which is coupled to the data output port of the PHY device so as to receive the program code transmitted by the code server in order to program the field-programmable logic device, and comprising a data input port, which is separate from the configuration port and is also coupled to the data output port of the PHY device so as to receive communication data transmitted over the network following conclusion of the programming phase, whereupon the field programmable logic device is programmed by the program code to process the communication data in accordance with a predetermined data link layer protocol.

11. (Previously presented) The apparatus according to claim 10, wherein the network node comprises no non-volatile memory for holding the program code.

12. (Previously presented) The apparatus according to claim 10, wherein the configuration port and data input port are connected in parallel to the data output port without other logic components intervening between the ports.

13. (Original) The apparatus according to claim 10, wherein the physical layer protocol and data link layer protocol comprise Ethernet protocols.

14. (Original) The apparatus according to claim 10, wherein the code server is adapted to frame the program code in data frames in accordance with the physical layer protocol, so as to cause the PHY device to output the program code through the data output port in a format suitable for programming the field programmable logic device.

15. (Original) The apparatus according to claim 14, wherein the code server is adapted to incorporate in the data frames, together with the program code, a sequence of clock bits, and wherein the field programmable logic device comprises a clock input, which is coupled to receive the clock bits from the PHY device so as to clock the program code into the configuration port.

16. (Original) The apparatus according to claim 10, wherein the field programmable logic device further comprises a data transmit port and is further programmed by the program code to generate data frames at the data transmit port in accordance with the data link protocol, and

wherein the PHY device comprises a data receive port, which is coupled to the data transmit port so as to receive the data frames generated by the field programmable logic device for transmission over the communication network via the network port.

17. (Original) The apparatus according to claim 10, wherein the field programmable logic device comprises a field programmable gate array (FPGA).

18. (Original) The apparatus according to claim 10, wherein the network node comprises an identification (ID) component holding an identification value and coupled to be read by the field programmable logic device, so that when the field programmable logic device is programmed by the program code, the network node conveys the identification value over the network to the code server.

19. (Original) The apparatus according to claim 18, wherein the program code comprises start-up program code and operational program code, wherein code server is adapted to initially transmit the start-up program code to the network node, causing the network node to convey the identification value over the network to the code server, and wherein the code server is further adapted, upon receiving the identification value, to select the operational program code to transmit to the network node responsively to the identification value.

20. (Currently amended) A method for network communication, comprising:

coupling a node, which comprises a programmable processor and a physical layer interface (PHY) device, to receive signals from a communication network via a network port of the PHY device;

processing the signals at the node in accordance with a predetermined physical layer protocol so as to generate a digital data output at a data output port of the PHY device;

transmitting the signals on the network in accordance with the physical layer protocol during a programming phase of the network so as to convey program code to the node;

coupling the data output port of the PHY device to a configuration port of the programmable processor, so as to program the processor using the transmitted program code;

following conclusion of the programming phase, transmitting the signals on the network in accordance with the physical layer protocol and with a predetermined data link layer protocol so as to convey communication data over the network to the node; and

coupling the data output port of the PHY device to a data input port of the programmable processor, which is separate from the configuration port, so that following the conclusion of the programming phase, the processor processes the communication data, responsively to the program code, in accordance with the data link layer protocol.

21. (Previously presented) The method according to claim 20, wherein the node comprises no non-volatile memory for holding the program code.

22. (Original) The method according to claim 20, wherein coupling the digital data output to the configuration port comprises connecting the configuration port and the data input port in parallel to receive the digital data output.

23. (Previously presented) The method according to claim 22, wherein connecting the configuration port and the data input port in parallel comprises connecting

the configuration port and the data input port without other logic components intervening between the ports.

24. (Original) The method according to claim 20, wherein the physical layer protocol and data link layer protocol comprise Ethernet protocols.

25. (Original) The method according to claim 24, wherein processing the signals comprises generating the digital data output in accordance with an Ethernet media independent interface (MII).

26. (Original) The method according to claim 20, wherein transmitting the signals during the programming phase comprises framing the program code in data frames in accordance with the physical layer protocol so as to cause a physical layer interface (PHY) device at the node to generate the digital data output in a format suitable for programming the programmable processor.

27. (Original) The method according to claim 26, wherein framing the program code comprises incorporating in the data frames, together with the program code, a sequence of clock bits, so as to cause the PHY device to generate a clock input to the programmable processor for clocking the program code into the configuration port.

28. (Original) The method according to claim 20, wherein the program code further causes the programmable processor to generate data frames in accordance with the data link protocol for transmission over the communication network.

29. (Original) The method according to claim 20, wherein the programmable processor comprises a field programmable gate array (FPGA).

30. (Original) The method according to claim 20, wherein the node comprises an identification (ID) component holding an identification value and coupled to be read by the programmable processor, and wherein transmitting the signals during the programming phase comprises:

initially transmitting start-up program code to the network node, causing the programmable processor to convey the identification value over the network to the code server;

receiving the identification value from the node; and

selecting operational program code to transmit to the node, responsively to the identification value, so as to cause the processor to processes the communication data, responsively to the operational program code, in accordance with the data link layer protocol.